WHAT IS CLAIMED IS:

1. A circuit, for driving a flat panel display, for receiving a data of a current source, a first signal and a second signal and outputting a current via a current output terminal, the circuit comprises:

a storage capacitor, having a first terminal and a second terminal, the first terminal being coupled to a system voltage, the second terminal being coupled to a storage voltage;

a transmission gate, comprising a first N-type transistor and a first P-type transistor, a first source/drain terminal of the first N-type transistor being coupled to a first source/drain terminal of the first P-type transistor serving as a first input/output terminal of the transmission gate, a second source/drain terminal of the first N-type transistor being coupled to a second source/drain terminal of the first P-type transistor serving as a second input/output terminal of the transmission gate, a gate terminal of the first N-type transistor being a first gate terminal of the transmission gate, a gate terminal of the first P-type transistor being a second gate terminal of the transmission gate, the first input/output terminal of the transmission gate being coupled to the storage voltage, the second input/output terminal of the transmission gate being coupled to the data current source, the first gate terminal of the transmission gate being coupled to the first signal, the second gate terminal of the transmission gate being coupled to the second signal; and

a current-limiting transistor, wherein a gate terminal of the current-limiting transistor is coupled to the storage voltage, a first source/drain terminal of the current-limiting transistor is coupled to the system voltage, a second source/drain terminal of

the current-limiting transistor is coupled to the current output terminal for determining current flow from the current-limiting transistor according to the storage voltage.

2. The circuit as recited in claim **1**, further comprises:

a second P-type transistor, for coupling the transmission gate to the data of the current source, a gate terminal of the second P-type transistor being coupled to the second signal; and

a second N-type transistor, for coupling the current-limiting transistor to the current output terminal, a gate terminal of the second N-type transistor being coupled to the second signal, wherein a terminal coupling the second N-type transistor and the limiting transistor is further coupled to the second input/output terminal of the transmission gate.

3. The circuit as recited in claim **1**, further comprises:

a second N-type transistor, coupling the transmission gate and the data of the current source, a gate terminal of the second N-type transistor being coupled to a third signal; and

a second P-type transistor, a first source/drain terminal of the second P-type transistor being coupled to the system voltage, a second source/drain terminal of the second P-type transistor being coupled to the second input/output terminal of the transmission gate, a gate terminal of the second P-type transistor being coupled to the storage voltage.

4. The circuit as recited in claim **1**, further comprises:

a second N-type transistor, for coupling the system voltage to the current limiting transistor, a gate terminal of the second N-type transistor being coupled to the system voltage; and

a third N-type transistor, a first source/drain terminal of the third P-type transistor being coupled to a first source/drain terminal of the current limiting transistor, a second source/drain terminal of the third P-type transistor being coupled to the data current source, a gate terminal of the third P-type transistor being coupled to the first signal.

5. The circuit as recited in claim **1**, further comprises:

a second P-type transistor, for coupling the transmission gate and the data current source, a gate terminal of the second P-type transistor being coupled to the second signal; and

a third P-type transistor, for coupling the current limiting transistor to the current output terminal, a gate terminal of the third P-type transistor being coupled to a third signal, wherein a terminal is coupled to the third P-type transistor and the current-limiting transistor is coupled to the second input/output transmission gate.

6. The circuit as recited in claim **1**, further comprising:

a second P-type transistor, for coupling the transmission gate to the data current source, a gate terminal of the second P-type transistor being coupled to the second signal; and

a third P-type transistor, wherein a first source/drain of the third P-type transistor is coupled to the system voltage, a second source/drain and a gate of the third P-type transistor are coupled to the second input/output terminal of the transmission gate.

7. The circuit as recited in claim **1**, wherein the first signal is inverse of the second signal.

8. The circuit as recited in claim **1**, wherein the flat panel display is an Organic Luminescence Emitting Display (OLED).

9. A circuit for driving a flat-panel display, for receiving a data of the current source, a first signal and a second signal and outputting a current via a current output terminal, the circuit comprises:

a storage capacitor, having a first terminal and a second terminal, the first terminal being coupled to a system voltage, the second terminal being coupled to a storage voltage;

a transmission gate, comprising a N-type transistor and a first P-type transistor, a first source/drain terminal of the N-type transistor being coupled to a first source/drain terminal of the first P-type transistor serving as a first input/output terminal of the transmission gate, a second source/drain terminal of the N-type transistor being coupling to the second source/drain terminal of the first P-type transistor serving as a second input/terminal of the transmission gate, a gate terminal of the N-type transistor being a first gate terminal of the transmission gate, a gate of the first P-type transistor being a second gate terminal of the transmission gate, the first input/output terminal of the transmission gate being coupled to the storage voltage, the first gate terminal of the transmission gate being coupled to the first signal, the second gate terminal of the transmission gate being coupled to the second signal;

a current-limiting transistor, wherein a gate terminal of the current-limiting transistor is coupled to the storage voltage, a first source/drain terminal of the current-limiting transistor is coupled to the system voltage for determining a current density flowing from the current-limiting transistor according to the storage voltage;

a second P-type transistor, wherein a first source/drain terminal of the second P-type transistor is coupled to the second input/output terminal of the transmission gate and a second source/drain terminal of the current-limiting transistor, a second

source/drain terminal of the second P-type transistor is coupled to the current output terminal;

a third P-type transistor, wherein a first source/drain terminal of the third P-type transistor is coupled to the storage voltage, and a second source/drain terminal and a gate terminal of the third P-type transistor are coupled to a gate of the second P-type transistor; and

a fourth P-type transistor, wherein a first source/drain terminal of the fourth P-type transistor is coupled to a gate of the third P-type transistor, a second source/drain terminal of the fourth P-type transistor is coupled to the data current source, and a gate of the fourth P-type transistor is coupled to the second signal.

10. The circuit as recited in claim 9, wherein the first signal is inverse of the second signal.

11. The circuit as recited in claim 9, wherein the flat panel display is an Organic Luminescence Emitting Display (OLED).